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MPC8xx I²C/SPI and SMC Relocation Microcode Packages

1 Overview

The modified I²C/SPI/SMC programming model allows concurrent operation of such SCC modes as Ethernet, QMC, and SMC/I²C/SPI by solving the parameter RAM (PRAM) conflict caused when some SCC parameters overlay the SMC/I²C/SPI parameters. This solution maps the SMC/I²C/SPI parameters to relocatable PRAM in the dual-ported RAM (DPRAM) area. Consult the chapter on the SCC in the *MPC860 PowerQUICC™ User's Manual* (MPC860UM) for details on parameter RAM.

2 Microcode Revision Numbers

The MPC8xx part and mask set number information is located in the internal memory map register (IMMR). The part number (PARTNUM) is IMMR[16–23]. The mask set number (MASKNUM) is IMMR[24–31].

The communications processor (CP) ROM microcode revision is stored to a half-word location called REV_NUM that resides in the "miscellaneous" section of the PRAM in DPRAM. REV_NUM is located at IMMR[0–15] + DPRAM base + 0x1CB0.

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3 Applicable MPC8xx Revisions

The I²C/SPI microcode package applies to all mask sets of the MPC850 family and to all mask sets of the MPC860 family up to Revision D.4. Revision D.4 (PARTNUM = 0x05, MASKNUM = 0x02, REV_NUM = 0x0000) is the last version of the MPC860 for which this package is relevant. The I²C/SPI relocation feature is integrated into the ROM microcode and is available on all MPC862, MPC866, and MPC885 family members.

The SMC relocation microcode package applies to all MPC8xx families and revisions. Note that SMC parameters can only be relocated in UART mode. Relocation of an SMC in Transparent or GCI mode is not supported.

4 Available Microcode Combinations

Four different combinations of microcode packages are available:

- I²C/SPI relocation
- SMC/SPI relocation
- SMC/I²C relocation
- SMC relocation

Use of microcode files depends on the chip revision, as shown in Table 1. If you cannot find your chip revision, contact Freescale support. The individual packages are identified by appropriate file names.

Table 1. Mapping Microcode File to Chip Revision

	MPC850 Family	MPC860SR Rev B.1	MPC 823	MPC823e	All other MPC860 parts	MPC862 Family <= Rev B	MPC866 Family >= Rev A	MPC885 Family <= Rev 0
850_i2c_spi	X	X	—	—	—	—	—	—
850_smc_spi	X	X	—	—	—	—	—	—
850_smc_i2c	X	X	—	—	—	—	—	—
850_smc	X	X	—	—	—	—	—	—
860_i2c_spi	—	—	X	X	X	—	—	—
860_smc_spi	—	—	X	X	X	—	—	—
860_smc_i2c	—	—	X	X	X	—	—	—
860_smc	—	—	X	X	X	X	X	X

5 Programming Model for SMC Relocation

The modified SMC (UART) programming model allows concurrent operation of Ethernet and SMC (UART) by solving the parameter RAM conflict caused when some Ethernet parameters overlay the SMC (UART) parameters. This solution maps the SMC (UART) parameters to other dual-ported RAM areas (relocatable parameter RAM).

RPBASE (Table 2) is a pointer to a 56-byte block in the DRAM. The RPBASE parameter value is valid only for the SMC microcode package. This parameter is not discussed in any other MPC8xx documentation. This parameter is a half-word field located at the 0x3C offset from the original SMC PRAM base. If both SMCs are to be used, both RPBASE parameters must be set up, even if one of the SMCs is effectively not relocated. The block to which each RPBASE points contains the actual SMC parameters in the same relative locations and order as in the original PRAM definition (Table 3). RPBASE should be divisible by 64. The relocatable PRAM values marked in boldface must be initialized by the user before the channel is enabled.

Table 2. RPBASE Location in Memory Map

Address	Name	Width	Description
SMC Base + 3C	**RPBASE**	Half word	Relocatable parameter RAM base

Table 3. SMC Parameter RAM Map

Address	Name	Width	Description	Comment
RPBASE + 00	**RBASE**	Half word	Rx BD base address	
RPBASE + 02	**TBASE**	Half word	Tx BD base address	
RPBASE + 04	**RFCR**	Byte	Rx function code	
RPBASE + 05	**TFCR**	Byte	Tx function code	
RPBASE + 06	**MRBLR**	Half word	Maximum receive buffer length	
RPBASE + 08	**RSTATE**	Word	Rx internal state	Initialize to zero.
RPBASE + 0C	—	Word	Rx internal data pntr	
RPBASE + 10	**RBPTR**	Half word	Rx BD pointer	Initialize to RBASE.
RPBASE + 12	—	Half word	Rx internal byte cnt	
RPBASE + 14	—	Word	Rx temp	
RPBASE + 18	**TSTATE**	Word	Tx internal state	Initialize to zero.
RPBASE + 1C	—	Word	Tx internal data pntr	
RPBASE + 20	**TBPTR**	Half word	Tx BD pointer	Initialize to TBASE.
RPBASE + 22	—	Half word	Tx internal byte cnt	
RPBASE + 24	—	Word	Tx temp	
RPBASE + 28	**MAX_IDL**	Half word	Maximum idle characters	

Table 3. SMC Parameter RAM Map (continued)

Address	Name	Width	Description	Comment
RPBASE + 2A	IDLC	Half word		
RPBASE + 2C	BRKLN	Half word		
RPBASE + 2E	**BRKEC**	Half word	Receive break condition counter	
RPBASE + 30	**BRKCR**	Half word	Break count register	
RPBASE + 32	R_MASK	Half word		
RPBASE + 34	—	Word	SDMA Temp	

6 Programming Model for I²C/SPI Relocation

The I²C and SPI PRAM memory maps are identical. When the SCC Ethernet is enabled, the original I²C/SPI PRAM is overlaid with the SCC Ethernet PRAM. Therefore, the original I²C or SPI PRAM is unusable. RPBASE (Table 4) is a pointer to a 40-byte block in the DRAM. The RPBASE parameter value is valid only for the I²C/SPI microcode package. This parameter is not discussed in any other MPC8xx documentation, except for the MPC862, MPC866, and MPC885 families. The RPBASE parameter is a half-word field located at 0x2C offset from the original I²C or SPI PRAM base. If both I²C and SPI are to be relocated, there must be one RPBASE for each block of PRAM. The block to which each RPBASE points contains the I²C/SPI parameters in the same relative locations and order as in the original PRAM definition (Table 5). RPBASE should be divisible by 32. The relocatable PRAM values marked in boldface must be initialized by the user before the channel is enabled.

Table 4. RPBASE Location in Memory Map

Address	Name	Width	Description
I²C or SPI Base + 2C	**RPBASE**	Half word	Relocatable parameter RAM base

Table 5. I²C or SPI Parameter RAM Map

Address	Name	Width	Description	Comment
RPBASE + 00	RBASE	Half word	Rx BD base address	
RPBASE + 02	TBASE	Half word	Tx BD base address	
RPBASE + 04	RFCR	Byte	Rx function code	
RPBASE + 05	TFCR	Byte	Tx function code	
RPBASE + 06	MRBLR	Half word	Maximum receive buffer length	
RPBASE + 08	RSTATE	Word	Rx internal state	Initialize to zero.
RPBASE + 0C	—	Word	Rx internal data pntr	
RPBASE + 10	RBPTR	Half word	Rx BD pointer	Initialize to RBASE.
RPBASE + 12	—	Half word	Rx internal byte cnt	

Table 5. I²C or SPI Parameter RAM Map (continued)

Address	Name	Width	Description	Comment
RPBASE + 14	—	Word	Rx temp	
RPBASE + 18	TSTATE	Word	Tx internal state	Initialize to zero.
RPBASE + 1C	—	Word	Tx internal data pntr	
RPBASE + 20	TBPTR	Half word	Tx BD pointer	Initialize to TBASE.
RPBASE + 22	—	Half word	Tx internal byte cnt	
RPBASE + 24	—	Word	Tx temp	

7 Trap Settings and DPRAM Usage

The patches occupy the first 512–2048 bytes of the DPRAM and 256–512 bytes at the end of the first 4K. Before enabling the microcode with the RCCR and trap settings, load it into the appropriate DPRAM space.

Table 6. File Name to Trap Setting Mapping

	RCTR1	RCTR2	RCTR3	RCTR4	RCCR[ERAM]
850_i2c_spi	0x8028	0x802a	0x802c	0x802e	0x01 (512+256)
850_smc_spi	0x8080	See Table 7	0x8028	0x802a	0x03 (2048+512)
850_smc_i2c	0x8080	See Table 7	0x802c	0x802e	0x03 (2048+512)
850_smc	0x8080	See Table 7	—	—	0x02 (1024+256)
860_i2c_spi	0x8028	0x802a	0x802c	0x802e	0x01 (512+256)
860_smc_spi	0x8080	See Table 7	0x8028	0x802a	0x03 (2048+512)
860_smc_i2c	0x8080	See Table 7	0x802c	0x802e	0x03 (2048+512)
860_smc	0x8080	See Table 7	—	—	0x02 (1024+256)

Table 7. Trap Values for SMC Relocation per Chip Type

	RCTR2
MPC821, all revisions	0x808A
MPC823, all revisions	0x808A
MPC823e, all revisions	0x808A

Table 7. Trap Values for SMC Relocation per Chip Type (continued)

	RCTR2
MPC860 Family, revision B and C non-SR parts	0x808A
All other MPC8xx	0x8088

8 Technical Notes

- If any SMC, I²C, or SPI parameters are relocated to a different address using the microcode patch, then all corresponding CPM host commands issued via the CP command register—for example, INIT_RX_AND_TX_PARAMS, STOP_TX, CLOSE_RX_BD—cannot be used in conjunction with the microcode patch. For an SMC, I²C, or SPI that is still configured to the original address space, the CPM commands can still be used.
- Trap settings differ for the different packages. Take care to use the correct set of settings.
- QMC channel-specific parameters occupy 64 bytes of DPRAM per channel. The I²C/SPI microcode package locks the first 512 bytes and the last 256 bytes at the end of the first 4 KB of the DPRAM. Therefore, support is lost for 12 of the possible 64 channels for I²C/SPI relocation. For any package with SMC relocation, 20 QMC channels are lost because the patch requires 1 KB at the beginning of the DPRAM. For the combined patch, 40 QMC channels are lost.

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