
LAN8670/1/2 Configuration Application Note

INTRODUCTION

This application note provides guidance on how to configure the LAN8670/1/2 Ethernet PHY for optimal performance in 10BASE-T1S networks.

REFERENCES

This application note is intended to be used in conjunction with the following documents:

LAN8670/1/2: 10BASE-T1S Ethernet PHY Transceiver Data Sheet

CONFIGURATION PROCESS

The configuration settings for the LAN8670/1/2 consist of a series of configuration register accesses performed through the Serial Management Interface (SMI). The register accesses are written immediately following reset of the device and should be performed in the sequence provided in this application note. Details for accessing the configuration registers through the SMI may be found in the device data sheet.

The types of register functions utilized in the configuration include:

- W – Write of value to specified register
- RMW – Read-Modified Write composed of a read of specified register, followed by a write of the logical AND of the value and mask to the specified register

The Read-Modified Write (RMW) register access, shown in pseudocode below, is used to write only specific register bit fields without unintended changes to other bits.

Read-Modified Write Pseudocode

```
current_val = read_register(mmd, addr) // Read current register value
new_val = current_val AND (NOT mask) // Clear bit fields to be written
new_val = new_val OR value // Set bits
write_register(mmd, addr, new_val) // Write back updated register value
```

where:

mmd MDIO Managed Device address of register
address Address of the register to access
value Value to be written to the register located in mmd at address
mask Mask with bits set to one which should be written

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CONFIGURATION SETTINGS FOR PRODUCT REVISION B1

The following configuration sequence applies to the LAN8670/1/2 hardware revisions listed in the following table.

Part Number	Part ID ¹	Hardware Revision ¹	Package Marking ²
LAN8670	010110	0010	B1
LAN8671	010110	0010	B1
LAN8672	010110	0010	B1

Note 1: The Part ID and Hardware Revision are located in the PHY_ID1 register Model Number and Revision Number fields, respectively.

2: Refer to the device Data Sheet for identification of the product revision on the package marking.

<u>Access</u>	<u>MMD</u>	<u>Address</u>	<u>Value</u>	<u>Mask</u>
RMW	0x1F	0x00D0	0x0002	0x0E03
RMW	0x1F	0x00D1	0x0000	0x0300
RMW	0x1F	0x0084	0x3380	0xFFC0
RMW	0x1F	0x0085	0x0006	0x000F
RMW	0x1F	0x008A	0xC000	0xF800
RMW	0x1F	0x0087	0x801C	0x801C
RMW	0x1F	0x0088	0x033F	0x1FFF
W	0x1F	0x008B	0x0404	-
RMW	0x1F	0x0080	0x0600	0x0600
RMW	0x1F	0x00F1	0x2400	0x7F00
RMW	0x1F	0x0096	0x2000	0x2000
W	0x1F	0x0099	0x7F80	-

APPENDIX A: APPLICATION NOTE REVISION HISTORY

A.1 Current Document Revision

Revision A (DS60001699A - July 2021)

- Initial Release

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